20.7 A 10.8mA Single Chip Transceiver for 430MHz Narrowband Systems in 0.15µm CMOS

George Hayashi[1], Akihiro Sawada[1], Takashi Morie[1], Kazuhiro Matsuyama[1], Ryangsu Kim[1], Seichiro Yoshida[1], Akinori Matsumoto[1], Katsumasa Hijikata[1], Kazuo Matsukawa[1], Yoshihiro Tamura[2], Jun Ogawa[2], Toshio Takita[2]

[1]Matsushita Electric Industrial, Osaka, Japan
[2]Panasonic Semiconductor Systems and Technology, Kyoto, Japan

Low-data-rate and narrowband wireless systems operating in the license-free ISM band at 430MHz are suitable for sensor networks and home security networks. These applications require low power, low cost, and small size transceiver. In particular, low power is strictly demanded for battery longevity, e.g., over 10 years with a lithium battery. To achieve such a requirement, the current draw of the receiver is desired to be under 12mA with the operating voltage of 2.0 to 3.5V, because the receive mode is dominant operation in these applications. However, previously reported CMOS transceivers for 430MHz narrowband systems consume more than 17mA and operate from a supply that is more than 2.2V [1].

In this paper, a low-power single-chip transceiver for 430MHz narrowband systems is described that can handle channel spacing as low as 12.5kHz. The transceiver is implemented in a 0.15µm CMOS process and integrates a radio, an image-rejection filter, a channel-select filter, a synthesizer loop filter, a digital demodulator, and a microcontroller. It supports 2/4FSK modulation formats at data rates from 2.4 up to 14.4kb/s. The block diagram of the transceiver is shown in Fig. 20.7.1. No off-chip filter such as SAW and ceramic filters is used. Only a few external components such as decoupling capacitors, crystal oscillators, and matching networks are used. A 180kHz low-IF receiver architecture and a direct-modulation transmitter are used for low-power and low-cost implementation. Each block uses low-threshold transistor (V_t=0.3V) for low-voltage operation and is biased by a regulator to improve PSRR.

Figure 20.7.2 shows the analog front-end circuits of the transceiver. The LNA is based on an inductively degenerated topology and the down-conversion IQ mixer is based on a single-balanced mixer. An LNA is typically a current hungry block therefore, the single-ended topology is preferable for low-power operation. The LNA/mixer circuitry draws a total current of 0.8mA. To suppress the digital noise, the clock of the digital block should be as low as possible. Thus, the microcontroller runs at 1.44MHz. Moreover, to minimize the digital noise propagation, careful layout of the LNA is adopted with deep-nwell structure.

The PA of the transmitter consists of a variable-gain driver amplifier and a single-ended cascode amplifier. The PA operates in overdriven Class-B mode and provides output power in the range of -8dBm to 13dBm. The PA is biased at 1.8V produced by the regulator to achieve the robustness against hot-carrier degradation.

The frequency synthesizer is based on the fractional-N architecture controlled by a ΔΣ modulation to obtain a fine frequency resolution of 10Hz and fast lock time of <100µs. Moreover, the digitally controlled divider technique is used to achieve high-accuracy frequency modulation. In the transmit mode, the modulation data which determines the frequency deviation of the output signal is modulated in the ΔΣ modulation block, and directly controls the divider of the synthesizer. This technique makes it possible to realize 4FSK modulation, even if the frequency deviation is as low as 2.1kHz

The VCO consists of two cross-coupled complementary differential pairs loaded by an on-chip inductor, binary weighted capacitors, and MOS varactors. The VCO exhibits a tuning range of over 20% and oscillates at twice the receive and transmit frequency. The VCO output is divided by 2 and quadrature LO signals are generated. There is no tail current source in the VCO core to achieve low phase noise for high adjacent channel selectivity (ACS) and high adjacent channel power rejection (ACPR). This is because the flicker noise of the tail current is up-converted and deteriorates the phase noise of the VCO at low offset frequencies [2]. The measured phase noise of the synthesizer is -93dBc/Hz at 10kHz offset from the carrier and the lock-up time is 75µs.

In the receive section, the filter design is important for low power consumption. If the channel-select filter is implemented in analog domain for narrowband systems such as a 12.5kHz channel spacing, the quality factor of the filter should be higher than 10. However, such a high-Q filter draws a large current and has a large noise contribution. To achieve low power consumption, the filter is co-designed in both analog and digital domains. The role of the analog filter is image rejection and anti-alias filtering for the ADC, and that of the digital filter is channel selection. Figure 20.7.3 shows the analog filter block diagram. The analog filter is implemented as a complex band-pass filter with 4th-order Butterworth characteristic centering at 180kHz, which provides 90kHz bandwidth and has more than 35dB image rejection ratio. The filter is based on a g_m-C architecture for low power consumption as compared with opamp type filters. The transconductor of g_m cell is based on an inverter type for large dynamic range. The filter block draws only 1.5mA. The filter has an internal automatic calibration circuit to adjust the frequency characteristics against process variation, which suppresses the deviation of filter bandwidth to less than 4%.

The filter output signal is amplified by the IF gain amplifier and digitized by the following 5.76MS/s band-pass ΔΣ ADC. The ΔΣ ADC relaxes the attenuation performance of the analog filter. The DR of 72dB is achieved by the ADC and the sufficient DR of the receiver is obtained without AGC loop in the entire receive chain. After the ADC, the 1b digital data stream is sent to the digital channel-select filter and digital FSK demodulator.

The transceiver is fabricated in a 0.15µm CMOS 1PS 5AL process with thick top metal and operates from a supply voltage of 2.0 to 3.5V. It integrates all the radio and digital building blocks. Figure 20.7.4 shows the measured selectivity characteristics of the transceiver. Without any external filters, the ACS and the jamming performance at 1MHz frequency offset are 45dB and 73dB, respectively. Figure 20.7.5 shows the PA output spectrum and eye diagram in 4FSK at 14.4kb/s data rate. The measured output power and ACPR are 10dBm and 47dBc, respectively. Measurement results are summarized in Fig. 20.7.6. The receiver current is 10.8mA. The transmitter draws 25.5mA with off-chip harmonic filter. The operation frequency is from 370 to 480MHz. A sensitivity of -120dBm at 1% BER has been achieved in 2FSK mode operating at 2.4kbps and the image rejection ratio is 35dB. The chip micrograph is shown in Fig. 20.7.7. The die area is 14.7mm^2. The chip performance is compatible with the ARIB STD-T67 for narrowband applications in Japan.

References:

[1] Philip Quinlan et al., "A Multimode 0.3–200-kb/s Transceiver for the 433/868/915-MHz Bands in 0.25µm CMOS," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp.2297-2310, Dec., 2004.

[2] Aly Ismail et al., "CMOS Differential LC Oscillator with Suppressed Up-Converted Flicker Noise," *ISSCC Dig. Tech. Papers*, pp. 258-259, Feb. 2005.

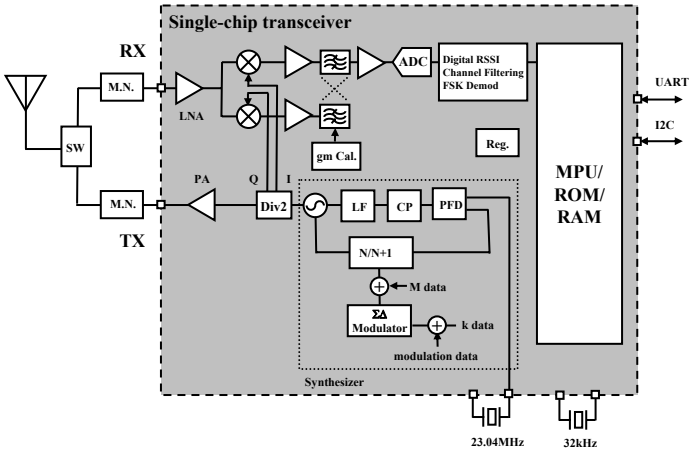

Figure 20.7.1: Transceiver block diagram.

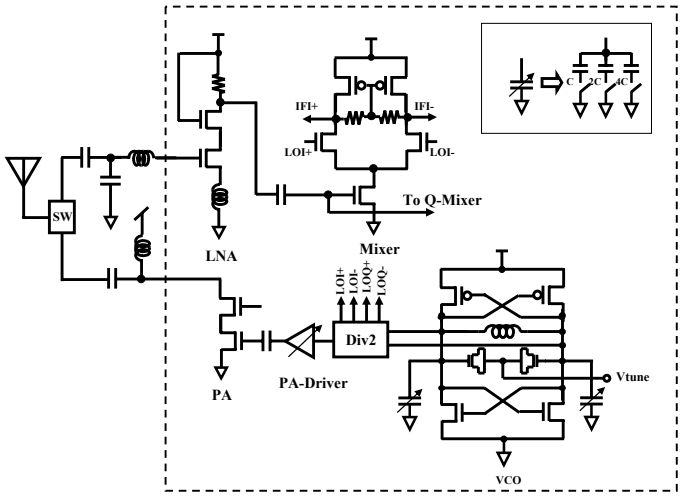

Figure 20.7.2: Analog front-end circuit.

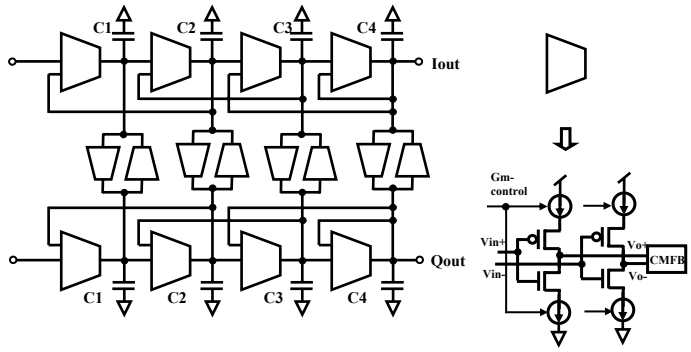

Figure 20.7.3: g_m-C filter circuit.

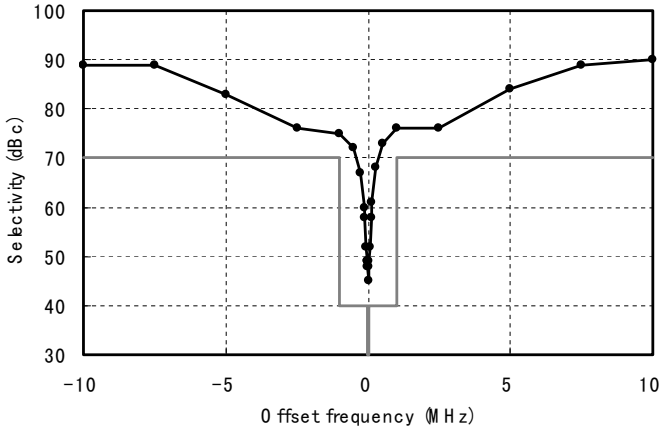

Figure 20.7.4: Measured selectivity characteristics.

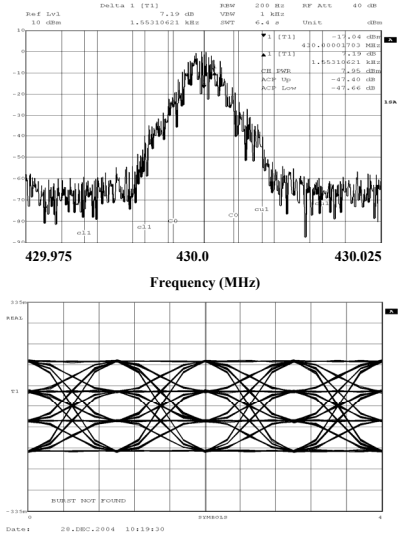

Figure 20.7.5: PA output spectrum and eye diagram in 4FSK at 14.4kb/s.

Vdd	2.0-3.5V
RX Idd	10.8mA
TX Idd	25.5mA, +10dBm
Halt Idd	2.5uA
Operating Frequency	370-480MHz
RX sensitivity 2.4kbps,FSK,fdev=2.1kHz	-120dBm
RX image Rejection 1% BER, Pin_min+3dB	35dB
RX Selectivity 1% BER, Pin_min+3dB	45dB ±12.5kHz(ACS) 73dB ±1MHz
Transmit Power	-8 to +13dBm
ACPR	50dBc, 2.4kb/s,2FSK,fdev=2.1kHz 47dBc, 14.4kb/s,4FSK,fdev=2.1kHz
Data Rate	2.4-14.4 kb/s
Die Area	14.7mm^2

Figure 20.7.6: Measured chip performances.

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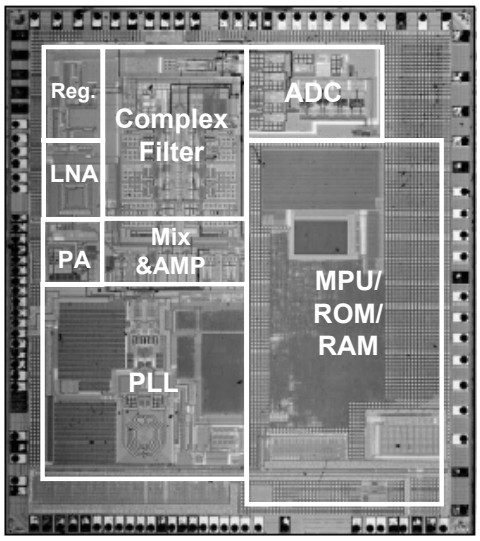

Figure 20.7.7: Die micrograph.

